Dynamic test of a batch of image sensors under thermal stress

Charlu TIZON$^{(a)}$, Kevin SANCHEZ$^{(b)}$, Rachel GRUNEISEN$^{(c),*}$

[a] BiBench Systems, 31 Allée Jules Guesdes, Le Village by CA, 31000 Toulouse, France

[b] C.N.E.S. (French Space Agency), 18 Avenue Edouard Belin, 31400 Toulouse, France

[c] Sodern (Ariane Group), 20 Avenue Descartes, 94450 Limeil-Brévannes, France

Abstract *This article presents two practical applications of functional tests of CMOS image sensors under thermal stress. Both experiments are based on the concept developed and patented by the French start-up BiBench. It allows a miniaturized and thermalized driver to be placed near the DUT, in the oven, without this driver being subject to thermal stress.*

The first application is for a scientific mission led by the CNES, which is the image sensor used on SuperCAM / Mars2020. The system allowed a continuous functional test of a small batch of sensors at high and low temperatures.

The second application takes place in an industrial context. It concerns the test of the image sensor from the star-tracker Auriga developed by Sodern. Auriga was notably selected Airbus OneWeb Satellites, with several thousand systems to be produced. Sodern and its partner AdvEOTec chose the Bibench equipment for repeated sets of electro-optical measurements at different stages of detector screening tests, including measures at high and low temperature. This sequence of measurements will be, in the end, performed over 150 times to cover the test of more than 2500 parts. The same equipment was also used during life test allowing the detectors to be submitted to 125°C while the proximity drivers remained thermalized.

The article details the concept of the system, the performed sequences and the advantages of this approach in terms of quality and efficiency.

Keywords: Image Sensor, Dynamic-Bun-In, Dynamic-Life-Test, Screening

1. INTRODUCTION

Everything starts with an inventory. For the vast majority of VLSI component aging tests, Burn-In, Life-Tests, are not performed with the 'functional' component, in the condition of its final use. Most often, electronic solutions exist to put it into operation “on the desk” but are too cumbersome or too expensive. Most importantly, they cannot be deported. This is a problem because in conventional Burn-in / Life-Test systems, the drivers are arranged at the rear of the oven, in a cold zone, and are too far away for high-speed signals. In addition, the number of connections available for each component is not sufficient to address each one individually.

As of today, there are solutions for carrying out these tests at lower ambient temperatures with heating sockets, but these require complex and expensive mechanical / thermal systems, specific for each type of component. This solution is not suitable for all components, in particular opto-electronic components.

From this inventory, two observations are made:

- Thanks to SoC, FPGA and the new generation of power supply components (HF DC / DC in particular), it is now possible to obtain drivers (power and signals) at reasonable cost and footprint. This enables monitoring a VLSI component, such as an image sensor, under actual operation.

- The simplest solution is to continue to carry out the test in an oven. In this case, it is necessary to design a system to cool the driver down and install it near the tested component.

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[*] *Corresponding author. e-mail : Charlu.tizon@bibench.com*

As the result of several years of R & D, the system exposed here is built on two essential concepts:

- A driver (power and signals) per component (or a small number of components). This driver is miniaturized to maintain a tested component density acceptable in terms of size. This driver must be versatile, reusable, and within an acceptable recurring cost.

Figure 1: 'Bibu1', the first version of the driver.

- An "air conditioning" system that allows the driver to be placed in the oven near the tested component.

The thermal solution proposed has been patented. The principle is to enclose the electronics in a thermally insulating housing, like a coffee thermos. A small flow of fresh air from outside circulates inside the housing to maintain the right temperature.

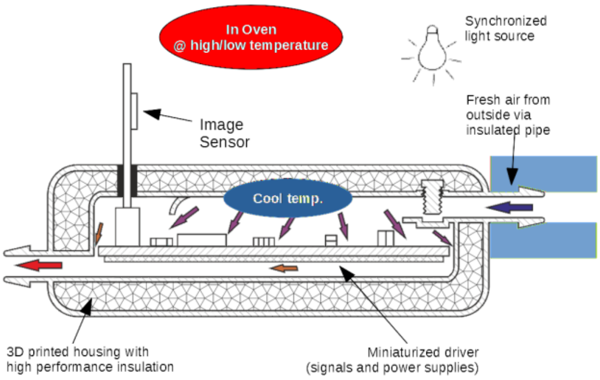

Figure 2: Patented thermal principle.

The housing is 3D printed, which gives the required level of flexibility to adapt to specific constraints (oven size, components form factor ...).

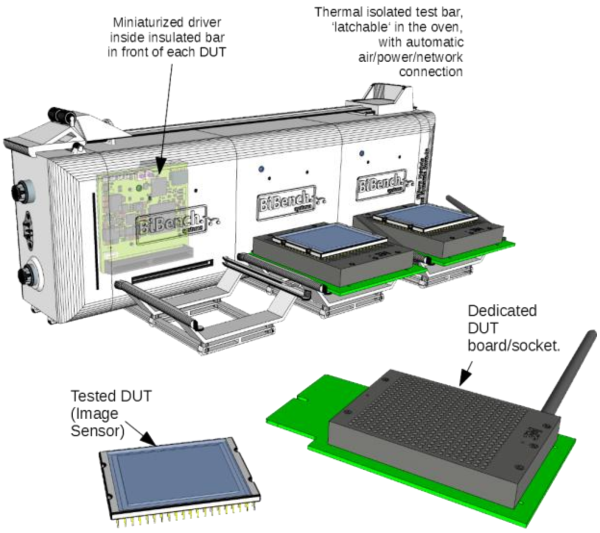

Figure 3: One DUT / One driver, 3 times…

The latest version of the system is in the form of a 'latchable' bar on a resident base in the oven, particularly easy to handle for operators.

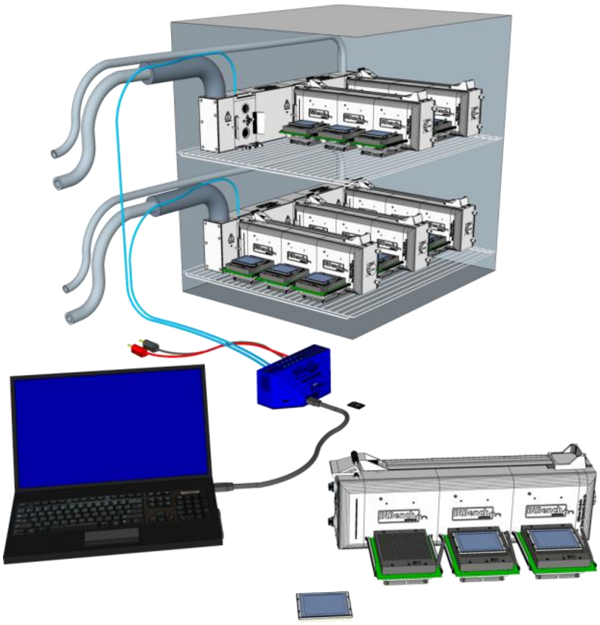

Figure 4: Complete system example.

2. FUNCTIONAL TEST UNDER TEMPERATURE STRESS OF THE SUPERCAM IMAGE SENSOR

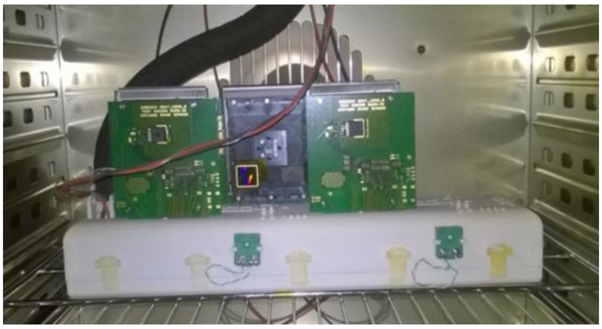

Figure 5: The three samples in the oven for high temperature test.

Since 2011, the CNES (DSO/AQ/LE) has been interested in Dynamic-Burn-In, Dynamic-Life-Test, and more generally, functional tests under thermal constraints and the contribution of this approach compared to conventional ones. Several campaigns have already taken place during the last years and have demonstrated the benefits of this approach.

It is in this context that the CNES wished to carry out during 2016 an evaluation of the operation under thermal stress, in real conditions and for a significant duration, of a few parts of the CMOSIS (now AMS) CMV4000 image sensors flight batch for SuperCAM / MARS2020. In addition to hot stress, a “cold campaign” has also been scheduled, according to the specifics of the mission. The goal was to validate the continuous operation of the sensor, without aberrant images, at high temperature (about 125 °C die) and low temperature (about -25 °C die), on a number of hours, similarly to Burn-In.

To put the sensor in nominal operation into an oven, while capturing images, is not an easy task. The first point to be able to objectively characterize an image, is to guarantee an adequate noise level on the power supplies, but also a reaction capacity (di / dt) avoiding the wave effect on the image. Only a fast power supply, implanted nearby, can guarantee such a result. Then, the other difficulty is the image acquisition itself. This is done on 16 serial links at 480Mbs, which is difficult to deport.

The test consisted of two campaigns of 168 hours each. The first one was done at 125 °C die (about 105 °C oven), and the second one at -25 °C die (-40 °C oven approx.). A synchronized light source was placed in the oven, allowing the 'light' and 'black' operation of the sensor. An exposure time control algorithm has been developed to put the sensor in a stable configuration for the ‘light’ phases of the test, whatever the temperature and drifts introduced by the sensor or light sources. The proposed algorithm ensures that the exposure time is kept within acceptable limits.

The sensors are in nominal operation at 48MHz (480Mbs output) and at the maximum frame rate (auto-chained mode).

The software of each driver makes the image acquisition on the fly (without storing it), by calculating a great number of parameters: number of pixels under/above thresholds (R, G, B), current consumption (max, min , avg), temperature (max, min, average acquired by THK or by the sensor itself via SPI), pixel values (min, max, avg) ... etc. Finally, 38 parameters are logged over the duration of the test.

Complementary tests were done by an Advantest V93000 parametric tester before and after tests in the oven to check and track any drifts.

The obtained results are satisfying, showing adequate operation of the sensor in any situation, and throughout the complete duration of the test.

This experience shows that the functional parameters of a high and low temperature VLSI component can be finely traced. The displayed curves exhibit some disparities from one sensor to another, and some drift in some parameters (such as the average value of the pixel in ‘black’ phase).

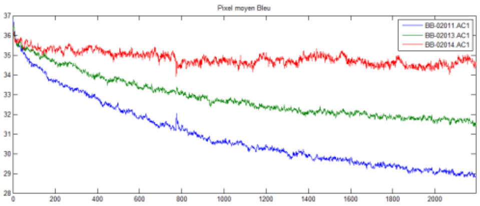

Figure 6: Drift of average pixel value in ‘black’ phase for blue pixels for the three samples.

In this case, everything remained in the norms, but we understand the interest of such curves in the case of a component that evolves in an unusual, or significantly different way from the others.

The experiment showed the relevance of this approach, as well as the usability and versatility of the system, since the same electronic base was used for a NAND FLASH component test in Dynamic-Life-Test.

3. DYNAMIC LIFE-TEST AND THERMAL SCREENING OF THE AURIGA IMAGE SENSOR

Description of the Sodern test set-up

The Bibench Systems benches have been extensively used to test the Auriga detectors. Auriga is Sodern’s latest-generation star tracker, designed for small satellites.

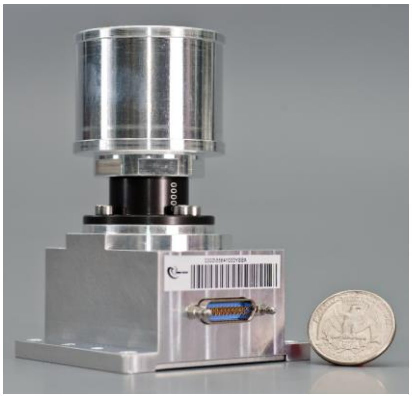

Figure 7: Sodern star tracker Auriga.

In the framework of the Auriga production and validation, Sodern performs space level screening, evaluation and lot acceptance tests on the detector according to the adhoc ESA ESCC generic specification. Screening is performed on a series of more than 2500 detectors.

These tests are defined by Sodern and performed by AdvEOTec. Life tests and screening initial, intermediate and final measurements are performed using the Bibench Systems test benches.

Due to the amount of detectors to be measured during screening tests, one test bar was required to operate four devices at a time and four such bars are used allowing to test sixteen devices simultaneously. The four benches are placed into a thermal chamber at AdvEOTec’s premises, also including light sources, to allow for measurements to be performed with or without illumination at high and low temperature (-40°C and +60°C) and at room temperature (25°C).

Two additional test benches were required for the evaluation and lot acceptance life tests, to bias several detectors at a 5 MHz clock rate (50Mbs output) for 2000 hours, at 125°C.

Figure 8: Bibench Systems test benches in thermal chamber at AdvEOTec’s.

The test benches, in addition to controlling the detector and the light sources, allow to calculate the mean signal of an image and the column Fixed Pattern Noise (FPN) in order to first determine the detector optimal working point. Sodern provided the processing software adapted to determine the parameters on which the detectors are then screened: dark current, dark signal non-uniformity, temporal noise and FPN, but also conversion factor, linearity and saturation, pixel response, non-uniformity responsivity and dead or hot pixels. Measurements necessitate the acquisition of multiple series of images, taken with light sources “off” or “on” at different detector integration times. Adveotec is managing the whole test sequencing through a specific batch.

Today, life tests are completed and the screening of the first series of 2500 detectors is over. Sodern gathered enough data to produce interesting statistics concerning the detector itself in terms of electro-optical characteristics as well as visual inspection and concerning the reliability of the Bibench Systems test benches.

Some results

The statistics on the detector parameters allowed to better define the outliers. Figure 9 shows the example of the full well capacity distribution. The upper limit has been determined to be around 11000 electrons.

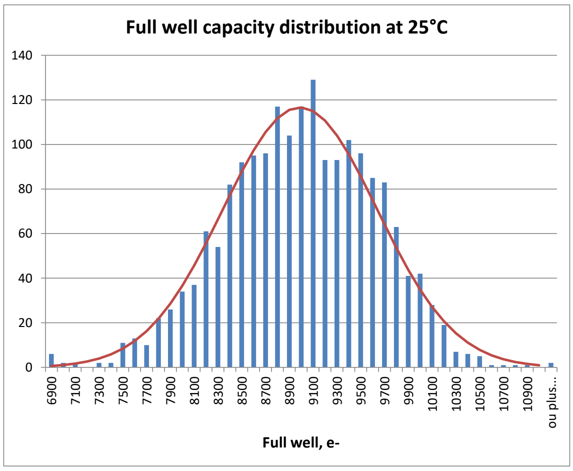

Figure 9: Distribution of the full well capacity.

Concerning the test bench, daughter boards on which the detectors are plugged suffered from oxidation after around 30 cycles. Therefore they were replaced by boards from a new manufacturer with a SnPb finish instead of the initial presumably too thin NiAu finish.

The next series of detectors will be tested using an upgraded test bench taking into account the first Auriga experience.

4. CONCLUSION

Through these two concrete experiences, the system has proven to be particularly suitable for image sensor testing: Dynamic-Burn-In, Dynamic-Life-Test or temperature screening. It allows multiple sensors to be functionally tested at full speed, possibly with a synchronized light source in the oven. It makes it possible to acquire and process images but also to trace the drifts of multiple optical and electrical parameters...

The system proves more efficient than previous approaches, offering a gain of time, and above all, an improvement of test quality.